	Digital Logic Design (CE and IT 3rd Semester) **Unit 1: Number Systems**
1	Any signed negative binary number is recognised by its _____ a) **MSB** b) LSB c) Byte d) Nibble
2	The representation of octal number (532.2)8 in decimal is _____ a) **(346.25)10** b) (532.864)10 c) (340.67)10 d) (531.668)10
3	The decimal equivalent of the binary number (1011.011)2 is _____ a) **(11.375)10** b) (10.123)10 c) (11.175)10 d) (9.23)10
4	An important drawback of binary system is _____ a) **It requires very large string of 1's and 0's to represent a decimal number** b) It requires sparingly small string of 1's and 0's to represent a decimal number c) It requires large string of 1's and small string of 0's to represent a decimal number d) It requires small string of 1's and large string of 0's to represent a decimal number
5	The decimal equivalent of the octal number (645)8 is _____ a) (450)10 b) (451)10 c) **(421)10** d) (501)10
6	The largest two digit hexadecimal number is _____ a) (FE)16 b) (FD)16 c) **(FF)16** d) (EF)16
7	Representation of hexadecimal number (6DE)H in decimal: a) **$6 * 16^2 + 13 * 16^1 + 14 * 16^0$** b) $6 * 16^2 + 12 * 16^1 + 13 * 16^0$ c) $6 * 16^2 + 11 * 16^1 + 14 * 16^0$ d) $6 * 16^2 + 14 * 16^1 + 15 * 16^0$
8	The given hexadecimal number (1E.53)16 is equivalent to _____ a) (35.684)8 b) **(36.246)8** c) (34.340)8 d) (35.599)8
9	The octal number (651.124)8 is equivalent to _____ a) **(1A9.2A)16** b) (1B0.10)16

	c) (1A8.A3)16 d) (1B0.B0)16
10	The octal equivalent of the decimal number (417)10 is _____ a) **(641)8** b) (619)8 c) (640)8 d) (598)8
11	Convert the hexadecimal number (1E2)16 to decimal: a) 480 b) 483 c) **482** d) 484
12	(170)10 is equivalent to a) (FD)16 b) (DF)16 c) **(AA)16** d) (AF)16
13	Convert (214)8 into decimal: a) **(140)10** b) (141)10 c) (142)10 d) (130)10
14	Convert (0.345)10 into an octal number: a) (0.16050)8 b) **(0.26050)8** c) (0.19450)8 d) (0.24040)8
15	Convert the binary number (01011.1011)2 into decimal: a) **(11.6875)10** b) (11.5874)10 c) (10.9876)10 d) (10.7893)10
16	Octal to binary conversion: (24)8 =? a) (111101)2 b) **(010100)2** c) (111100)2 d) (101010)2
17	Convert binary to octal: (110110001010)2 =? a) (5512)8 b) **(6612)8** c) (4532)8 d) (6745)8
18	What is the addition of the binary numbers 11011011010 and 010100101? a) 0111001000 b) 1100110110 c) **11101111111** d) 10011010011
19	Perform binary addition: 101101 + 011011 = ? a) 011010 b) 1010100

	c) 101110 d) **1001000**
20	Perform binary subtraction: 101111 – 010101 = ? a) 100100 b) 010101 **c) 011010** d) 011001
21	Binary subtraction of 100101 – 011110 is a) **000111** b) 111000 c) 010101 d) 101010
22	Perform multiplication of the binary numbers: 01001 × 01011 = ? a) **001100011** b) 110011100 c) 010100110 d) 101010111
23	100101 × 0110 = ? a) 1011001111 b) 0100110011 **c) 101111110** d) 0110100101
24	On multiplication of (10.10) and (01.01), we get a) 101.0010 b) 0010.101 c) **011.0010** d) 110.0011
25	Divide the binary numbers: 111101 ÷ 1001 and find the remainder a) 0010 b) 1010 c) 1100 **d) 0011**
26	Divide the binary number (011010000) by (0101) and find the quotient a) 100011 b) **101001** c) 110010 d) 010001
27	Binary subtraction of 101101 – 001011 = ? **a) 100010** b) 010110 c) 110101 d) 101100
28	1’s complement of 1011101 is _____ a) 0101110 b) 1001101 **c) 0100010** d) 1100101
29	2’s complement of 11001011 is _____ a) 01010111 b) 11010100

	c) 00110101 d) 11100010
30	If the number of bits in the sum exceeds the number of bits in each added numbers, it results in _____ a) Successor b) **Overflow** c) Underflow d) Predecessor
31	1's complement can be easily obtained by using _____ a) Comparator b) **Inverter** c) Adder d) Subtractor
32	The advantage of 2's complement system is that _____ a) **Only one arithmetic operation is required** b) Two arithmetic operations are required c) No arithmetic operations are required d) Different Arithmetic operations are required
33	The 1's complements requires _____ a**) One operation** b) Two operations c) Three operations d) Combined Operations
34	Which one is used for logical manipulations? a) 2's complement b) 9's complement c) **1's complement** d) 10's complement
35	For arithmetic operations only _____ a) 1's complement is used b) **2's complement** c) 10's complement d) 9's complement
36	Binary coded decimal is a combination of _____ a) Two binary digits b) Three binary digits c) **Four binary digits** d) Five binary digits
37	The decimal number 10 is represented in its BCD form as _____ a) 10100000 b) 01010111 c) **00010000** d) 00101011
38	Add the two BCD numbers: 1001 + 0100 = ? a) 10101111 b) 01010000 c) **00010011** d) 00101011
39	Code is a symbolic representation of _____ information. a) Continuous

	b) **Discrete** c) Analog d) Both continuous and discrete
40	When numbers, letters or words are represented by a special group of symbols, this process is called _____ a) Decoding b) **Encoding** c) Digitizing d) Inverting
41	The excess-3 code for 597 is given by _____ a) **100011001010** b) 100010100111 c) 010110010111 d) 010110101101
42	The decimal equivalent of the excess-3 number 110010100011.01110101 is _____ **a) 970.42** b) 1253.75 c) 861.75 d) 1132.87
43	Positive integers can be represented as A. Signed numbers **B. Unsigned numbers** C. Negative integers D. both A and B
44	Representation of -9 with signed magnitude equals to **A. 10001001** B. 11110110 C. 11110111 D. 11110011
45	The more convenient system for representing the negative numbers is **A. Signed-complement system** B. Unsigned-complement system C. Negative integer system D. Positive integer system
46	1's complement as a logical operation is equivalent to A. Logical design

	B. Illogical design **C. Logical complement** D. Illogical complement
47	The most commonly used system for representing signed binary numbers is the: **A. 2's-complement system.** **B.** 1's-complement system. **C.** 10's-complement system. **D.** sign-magnitude system.
48	The decimal value for E_{16} is: **A.** 12_{10} **B.** 13_{10} **C.** **14_{10}** **D.** 15_{10}
49	The binary subtraction 0 – 0 = **A.** **difference = 0** **borrow = 0** **B.** difference = 1 borrow = 0 **C.** difference = 1 borrow = 1 **D.** difference = 0 borrow = 1
50	Adding in binary, a decimal 26 + 27 will produce a sum of: **A.** 111010 **B.** 110110 **C.** **110101** **D.** 101011

	Unit 2: Boolean Algebra and Logic Gates
1	In boolean algebra, the OR operation is performed by which properties? a) Associative properties b) Commutative properties c) **Distributive properties** d) All of the Mentioned

2	The expression for Absorption law is given by _____ a) **A + AB = A** b) A + AB = B c) AB + AA’ = A d) A + B = B + A
3	According to boolean law: A + 1 = ? a) **1** b) A c) 0 d) A’
4	The involution of A is equal to _____ a) **A** b) A’ c) 1 d) 0
5	A(A + B) = ? a) AB b) 1 c) (1 + AB) **d) A**
6	DeMorgan’s theorem states that _____ **a) (AB)’ = A’ + B’** b) (A + B)’ = A’ * B c) A’ + B’ = A’B’ d) (AB)’ = A’ + B
7	(A + B)(A’ * B’) = ? a) 1 **b) 0** c) AB d) AB’
8	Complement of the expression A’B + CD’ is _____ a) (A’ + B)(C’ + D) **b) (A + B’)(C’ + D)** c) (A’ + B)(C’ + D) d) (A + B’)(C + D’)
9	Simplify Y = AB’ + (A’ + B)C. **a) AB’ + C** b) AB + AC c) A’B + AC’ d) AB + A
10	The boolean function A + BC is a reduced form of _____ a) AB + BC **b) (A + B)(A + C)** c) A’B + AB’C d) (A + C)B
11	The logical sum of two or more logical product terms is called _____ **a) SOP** b) POS c) OR operation d) NAND operation

12	The expression Y=AB+BC+AC shows the _____ operation. a) EX-OR **b) SOP** c) POS d) NOR
13	The expression Y=(A+B)(B+C)(C+A) shows the _____ operation. a) AND b) **POS** c) SOP d) NAND
14	A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____ **a) Minterm** b) Maxterm c) Midterm d) ∑ term
15	According to the property of minterm, how many combination will have value equal to 1 for K input variables? a) 0 **b) 1** c) 2 d) 3
16	The canonical sum of product form of the function y(A,B) = A + B is _____ a) AB + BB + A'A **b) AB + AB' + A'B** c) BA + BA' + A'B' d) AB' + A'B + A'B'
17	A variable on its own or in its complemented form is known as a _____ a) Product Term **b) Literal** c) Sum Term d) Word
18	Maxterm is the sum of _____ of the corresponding Minterm with its literal complemented. **a) Terms** b) Words c) Numbers d) Nibble
19	Canonical form is a unique way of representing _____ a) SOP b) Minterm **c) Boolean Expressions** d) POS
20	There are _____ Minterms for 3 variables (a, b, c). a) 0 b) 2 **c) 8** d) 1
21	_____ expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.

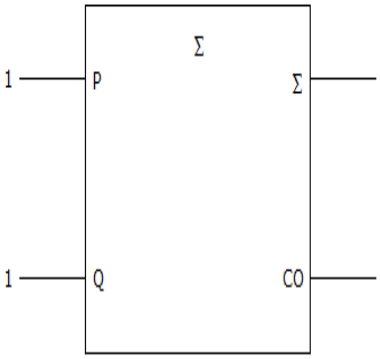
	a) POS b) Literals **c) SOP** d) POS
22	A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares. **a) Venn Diagram** b) Cycle Diagram c) Block diagram d) Triangular Diagram
23	There are _____ cells in a 4-variable K-map. a) 12 **b) 16** c) 18 d) 8
24	Each product term of a group, w'.x.y' and w.y, represents the _____in that group. a) Input b) POS **c) Sum-of-Minterms** d) Sum of Maxterms
25	Product-of-Sums expressions can be implemented using _____ a) 2-level OR-AND logic circuits b) 2-level NOR logic circuits c) 2-level XOR logic circuits **d) Both 2-level OR-AND and NOR logic circuits**
26	Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given _____ a) Function **b) Value** c) Set d) Word
27	Don't care conditions can be used for simplifying Boolean expressions in _____ a) Registers b) Terms **c) K-maps** d) Latches
28	Using the transformation method you can realize any POS realization of OR-AND with only. a) XOR b) NAND c) AND **d) NOR**
29	There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations. **a) X-NOR** b) XOR c) NOR d) NAND

30	These logic gates are widely used in _____ design and therefore are available in IC form. a) Sampling **b) Digital** c) Analog d) Systems
31	A single transistor can be used to build which of the following digital logic gates? a) AND gates b) OR gates c) **NOT gates** d) NAND gates
32	How many AND gates are required to realize Y = CD + EF + G? a) 4 b) 5 c) 3 **d) 2**
33	The NOR gate output will be high if the two inputs are _____ **a) 00** b) 01 c) 10 d) 11
34	How many two-input AND and OR gates are required to realize Y = CD+EF+G? **a) 2, 2** b) 2, 3 c) 3, 3 d) 3, 2
35	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate? a) OR b) AND c) XOR **d) NAND**
36	How many two input AND gates and two input OR gates are required to realize Y = BD + CE + AB? **a) 3, 2** b) 4, 2 c) 1, 1 d) 2, 3
37	Which of following are known as universal gates? **a) NAND & NOR** b) AND & OR c) XOR & OR d) EX-NOR & XOR
38	A single transistor can be used to build which of the following digital logic gates? a) AND gates b) OR gates **c) NOT gates** d) NAND gates
39	How many truth table entries are necessary for a four-input circuit? a) 4

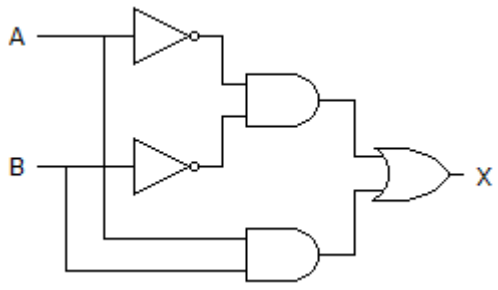
	b) 8 c) 12 **d) 16**
40	Which input values will cause an AND logic gate to produce a HIGH output? a) At least one input is HIGH b) At least one input is LOW **c) All inputs are HIGH** d) All inputs are LOW
41	Exclusive-OR (XOR) logic gates can be constructed from what other logic gates? a) OR gates only b) AND gates and NOT gates **c) AND gates, OR gates, and NOT gates** d) OR gates and NOT gates
42	The basic logic gate whose output is the complement of the input is the _____ a) OR gate b) AND gate **c) INVERTER gate** d) XOR gate
43	The AND function can be used to _____ and the OR function can be used to _____ **a) Enable, disable** b) Disable, enable c) Synchronize, energize d) Detect, invert
44	If we use an AND gate to inhibit a signal from passing one of the inputs must be _____ **a) LOW** b) HIGH c) Inverted d) Floating
45	Logic gate circuits contain predictable gate functions that open theirs _____ a) Outputs **b) Inputs** c) Pre-state d) Impedance state
46	How many NAND circuits are contained in a 7400 NAND IC? a) 1 b) 2 **c) 4** d) 8
47	The OR gate output will be LOW if the two inputs are _____ **a) 00** b) 01 c) 10 d) 11
48	The expression Y=(A+B) (B+C) shows the _____ operation. a) EX-OR b) SOP

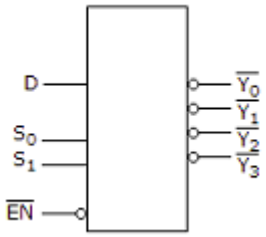
	c) POS d) NOR
49	There are _____ cells in a 3-variable K-map. a) 12 b) 16 c) 18 **d) 8**
50	There are _____ cells in a 2-variable K-map. a) 12 **b) 4** c) 18 d) 8

	Unit 3: Combinational Logic Design
1	A full adder logic circuit will have _____ a) Two inputs and one output b) Three inputs and three outputs c) Two inputs and two outputs **d) Three inputs and two outputs**
2	The gates required to build a half adder are _____ a) EX-OR gate and NOR gate b) EX-OR gate and OR gate **c) EX-OR gate and AND gate** d) EX-NOR gate and AND gate
3	What are the two types of basic adder circuits? **A.** sum and carry **B. half-adder and full-adder** **C.** asynchronous and synchronous **D.** one- and two's-complement
4	How many inputs must a full-adder have? **A.** 4 **B.** 2 **C.** 5 **D. 3**
5	Which of the statements below best describes the given figure?

	 **A. Half-carry adder; Sum = 0, Carry = 1** **B.** Half-carry adder; Sum = 1, Carry = 0 **C.** Full-carry adder; Sum = 1, Carry = 0 **D.** Full-carry adder; Sum = 1, Carry = 1
6	A full-adder adds _____. **A. two single bits and one carry bit** **B.** two 2-bit binary numbers **C.** two 4-bit binary numbers **D.** two 2-bit numbers and one carry bit
7	The basic building blocks of the arithmetic unit in a digital computers are _____ a) Subtractors **b) Adders** c) Multiplexer d) Comparator
8	A digital system consists of _____ types of circuits. **a) 2** b) 3 c) 4 d) 5
9	In a combinational circuit, the output at any time depends only on the _____ at that time. a) Voltage **b) Intermediate values** c) Input values d) Clock pulses
10	All logic operations can be obtained by means of _____ a) AND and NAND operations b) OR and NOR operations c) OR and NOT operations **d) NAND and NOR operations**
11	The design of an ALU is based on _____ a) Sequential logic

	b) Combinational logic c) Multiplexing d) De-Multiplexing
12	If the two numbers are unsigned, the bit conditions of interest are the _____ carry and a possible _____ result. a) Input, zero b) Output, one c) Input, one **d) Output, zero**
13	The flag bits in an ALU is defined as _____ a) The total number of registers **b) The status bit conditions** c) The total number of control lines d) All of the Mentioned
14	Total number of inputs in a half adder is _____ **a) 2** b) 3 c) 4 d) 1
15	In which operation carry is obtained? a) Subtraction **b) Addition** c) Multiplication d) Both addition and subtraction
16	If A and B are the inputs of a half adder, the sum is given by _____ a) A AND B b) A OR B **c) A XOR B** d) A EX-NOR B
17	If A and B are the inputs of a half adder, the carry is given by _____ **a) A AND B** b) A OR B c) A XOR B d) A EX-NOR B
18	The difference between half adder and full adder is _____ a) Half adder has two inputs while full adder has four inputs b) Half adder has one output while full adder has two outputs **c) Half adder has two inputs while full adder has three inputs** d) All of the Mentioned
19	If A, B and C are the inputs of a full adder then the sum is given by _____ a) A AND B AND C b) A OR B AND C **c) A XOR B XOR C** d) A OR B OR C
20	How many AND, OR and EXOR gates are required for the configuration of full adder? a) 1, 2, 2 **b) 2, 1, 2** c) 3, 1, 2 d) 4, 0, 1

21	Half subtractor is used to perform subtraction of _____ **a) 2 bits** b) 3 bits c) 4 bits d) 5 bits
22	For subtracting 1 from 0, we use to take a _____ from neighbouring bits. a) Carry **b) Borrow** c) Input d) Output
23	How many outputs are required for the implementation of a subtractor? a) 1 **b) 2** c) 3 d) 4
24	Let the input of a subtractor is A and B then what the output will be if A = B? **a) 0** b) 1 c) A d) B
25	Let A and B is the input of a subtractor then the output will be _____ **a) A XOR B** b) A AND B c) A OR B d) A EXNOR B
26	Full subtractor is used to perform subtraction of _____ a) 2 bits **b) 3 bits** c) 4 bits d) 8 bits
27	The output of a subtractor is given by (if A, B and X are the inputs). a) A AND B XOR X **b) A XOR B XOR X** c) A OR B NOR X d) A NOR B XOR X
28	The output of a full subtractor is same as _____ a) Half adder **b) Full adder** c) Half subtractor d) Decoder
29	Which of the following logic expressions represents the logic diagram shown? 

	a) X=AB'+A'B b) X=(AB)'+AB c) X=(AB)'+A'B' **d) X=A'B'+AB**
30	The device shown here is most likely a _____  a) Comparator b) Multiplexer c) Inverter **d) Demultiplexer**
31	3 bits full adder contains _____ a) 3 combinational inputs b) 4 combinational inputs c) 6 combinational inputs **d) 8 combinational inputs**
32	What is a multiplexer? a) It is a type of decoder which decodes several inputs and gives one output b) **A multiplexer is a device which converts many signals into one** c) It takes one input and results into many output d) It is a type of encoder which decodes several inputs and gives one output
33	What is the function of an enable input on a multiplexer chip? a) To apply Vcc b) To connect ground **c) To active the entire chip** d) To active one half of the chip
34	In a multiplexer, the selection of a particular input line is controlled by _____ a) Data controller **b) Selected lines** c) Logic gates d) Both data controller and selected lines
35	If the number of n selected input lines is equal to 2^m then it requires _____ select lines. a) 2 **b) m** c) n d) 2^n
36	How many select lines would be required for an 8-line-to-1-line multiplexer? a) 2 b) 4 c) 8 **d) 3**
37	How many NOT gates are required for the construction of a 4-to-1 multiplexer? a) 3

	b) 4 **c) 2** d) 5
38	In 1-to-4 demultiplexer, how many select lines are required? **a) 2** b) 3 c) 4 d) 5
39	How many AND gates are required for a 1-to-8 multiplexer? a) 2 b) 6 **c) 8** d) 5
40	How many OR gates are required for an octal-to-binary encoder? **a) 3** b) 2 c) 8 d) 10
41	Can an encoder be called as multiplexer? a) No **b) Yes** c) Sometimes d) Never
42	How many inputs are required for a 1-of-10 BCD decoder? **a) 4** b) 8 c) 10 d) 2
43	How many inputs are required for a 1-of-16 decoder? a) 2 b) 16 c) 8 **d) 4**
44	Reflected binary code is also known as _____ a) BCD code b) Binary code c) ASCII code **d) Gray Code**
45	Why do we use gray codes? a) To count the no of bits changes b) To rotate a shaft **c) Error correction** d) Error Detetction
46	Convert binary number into gray code: 100101. a) 101101 b) 001110 **c) 110111** d) 111001
47	One that is not the outcome of magnitude comparator is _____ a) a > b

	b) a – b c) a < b d) a = b
48	If two numbers are not equal then binary variable will be _____ **a) 0** b) 1 c) A d) B
49	In a comparator, if we get input as A>B then the output will be _____ **a) 1** b) 0 c) A d) B
50	Which one is a basic comparator? **a) XOR** b) XNOR c) AND d) NAND

	Unit 4: Sequential Circuits
1	In a sequential circuit, the output at any time depends only on the input values at that time. a) Past output values b) Intermediate values **c) Both past output and present input** d) Present input values
2	A latch is an example of a _____ a) Monostable multivibrator b) Astable multivibrator **c) Bistable multivibrator** d) 555 timer
3	Latch is a device with _____ a) One stable state **b) Two stable state** c) Three stable state d) Infinite stable states
4	Why latches are called a memory devices? a) It has capability to stare 8 bits of data b) It has internal memory of 4 bit **c) It can store one bit of data** d) It can store infinite amount of data
5	Two stable states of latches are _____ a) Astable & Monostable b) Low input & high output **c) High output & low output** d) Low output & high input
6	The full form of SR is _____ a) System rated **b) Set reset**

	c) Set ready d) Set Rated
7	The SR latch consists of _____ a) 1 input **b) 2 inputs** c) 3 inputs d) 4 inputs
8	The outputs of SR latch are _____ a) x and y b) a and b c) s and r **d) q and q'**
9	When both inputs of a J-K flip-flop cycle, the output will _____ a) Be invalid b) Change **c) Not change** d) Toggle
10	A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates? a) AND or OR gates b) XOR or XNOR gates **c) NOR or NAND gates** d) AND or NOR gates
11	Whose operations are more faster among the following? a) **Combinational circuits** b) Sequential circuits c) Latches d) Flip-flops
12	How many types of sequential circuits are? **a) 2** b) 3 c) 4 d) 5
13	The sequential circuit is also called _____ a) Flip-flop **b) Latch** c) Strobe d) Adder
14	The characteristic of J-K flip-flop is similar to _____ **a) S-R flip-flop** b) D flip-flop c) T flip-flop d) Gated T flip-flop
15	A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____ **a) Two AND gates** b) Two NAND gates c) Two NOT gates d) Two OR gates

16	How is a J-K flip-flop made to toggle? a) J = 0, K = 0 b) J = 1, K = 0 c) J = 0, K = 1 **d) J = 1, K = 1**
17	In J-K flip-flop, “no change” condition appears when _____ a) J = 1, K = 1 b) J = 1, K = 0 c) J = 0, K = 1 **d) J = 0, K = 0**
18	On a J-K flip-flop, when is the flip-flop in a hold condition? **a) J = 0, K = 0** b) J = 1, K = 0 c) J = 0, K = 1 d) J = 1, K = 1
19	How many types of flip-flops are? a) 2 b) 3 **c) 4** d) 5
20	The S-R flip flop consist of _____ a) 4 AND gates **b) Two additional AND gates** c) An additional clock input d) 3 AND gates
21	What is one disadvantage of an S-R flip-flop? a) It has no Enable input **b) It has a RACE condition** c) It has no clock input d) Invalid State
22	What is the hold condition of a flip-flop? a) Both S and R inputs activated **b) No active S or R input** c) Only S is active d) Only R is active
23	The characteristic of J-K flip-flop is similar to _____ **a) S-R flip-flop** b) D flip-flop c) T flip-flop d) Gated T flip-flop
24	In D flip-flop, D stands for _____ a) Distant **b) Data** c) Desired d) Delay
25	The D flip-flop has _____ input. **a) 1** b) 2 c) 3 d) 4

26	The D flip-flop has _____ output/outputs. **a) 2** b) 3 c) 4 d) 1
27	A D flip-flop can be constructed from an _____ flip-flop. **a) S-R** b) J-K c) T d) S-K
28	In D flip-flop, if clock input is HIGH & D=1, then output is _____ **a) 0** b) 1 c) Forbidden d) Toggle
29	In D flip-flop, if clock input is LOW, the D input _____ **a) Has no effect** b) Goes high c) Goes low d) Has effect
30	The characteristic equation of D-flip-flop implies that _____ a) The next state is dependent on previous state b) The next state is dependent on present state c) The next state is independent of previous state **d) The next state is independent of present state**
31	The asynchronous input can be used to set the flip-flop to the _____ a) 1 state b) 0 state **c) either 1 or 0 state** d) forbidden State
32	Input clock of RS flip-flop is given to _____ a) Input **b) Pulser** c) Output d) Master slave flip-flop
33	D flip-flop is a circuit having _____ a) 2 NAND gates b) 3 NAND gates **c) 4 NAND gates** d) 5 NAND gates
34	Master slave flip flop is also referred to as? a) Level triggered flip flop **b) Pulse triggered flip flop** c) Edge triggered flip flop d) Edge-Level triggered flip flop
35	In a positive edge triggered JK flip flop, a low J and low K produces? a) High state b) Low state c) Toggle state **d) No Change State**

36	Which of the following is the Universal Flip-flop? a) S-R flip-flop **b) J-K flip-flop** c) Master slave flip-flop d) D Flip-flop
37	Flip-flops are _____ a) Stable devices b) Astable devices **c) Bistable devices** d) Monostable devices
38	UP-DOWN counter is a combination of _____ a) Latches b) Flip-flops c) UP counter **d) Up counter & down counter**
39	In 4-bit up-down counter, how many flip-flops are required? a) 2 b) 3 **c) 4** d) 5
40	The register is a type of _____ **a) Sequential circuit** b) Combinational circuit c) CPU d) Latches
41	How many types of registers are? a) 2 b) 3 **c) 4** d) 5
42	The full form of SIPO is _____ **a) Serial-in Parallel-out** b) Parallel-in Serial-out c) Serial-in Serial-out d) Serial-In Peripheral-Out
43	A register is able to hold _____ a) Data **b) Word** c) Nibble d) Both data and word
44	The full form of ROM is _____ a) Read Outside Memory b) Read Out Memory **c) Read Only Memory** d) Read One Memory
45	ROM consist of _____ a) NOR and OR arrays b) NAND and NOR arrays **c) NAND and OR arrays** d) NOR and AND arrays

46	The full form of PROM is _____ a) Previous Read Only Memory b) Programmable Read Out Memory **c) Programmable Read Only Memory** d) Previous Read Out Memory
47	Which of the following comes under secondary memory/ies? a) Floppy disk b) Magnetic drum c) Hard disk **d) All of the Mentioned**
48	A Random Access Memory is one in which _____ a) Any location can be accessed sequentially **b) Any location can be accessed randomly** c) Any location can be accessed serially d) Any location can be accessed parallely
49	An example of RAM is _____ a) Floppy disk b) Hard disk c) Magnetic tape memory **d) Semiconductor RAM**
50	A static memory is one in which _____ a) Content changes with time b) Content doesn't changes with time c) Memory is static always **d) Memory is dynamic always**

	Unit 5: Register Transfer Logic
1	CPU has built-in ability to execute a particular set of machine instructions, called as _____ **a) Instruction Set** b) Registers c) Sequence Set d) User instructions
2	The length of a register is called _____ a) word limit **b) word size** c) register limit d) register size
3	The _____ holds the contents of the accessed memory word. a) MAR **b) MBR** c) PC d) IR
4	Which of the following is not a visible register? a) General Purpose Registers b) Address Register c) Status Register **d) MAR**

5	Which of the following is a data transfer instruction? **a) STA 16-bit address** b) ADD A, B c) MUL C, D d) RET
6	What is correct instruction if you want the control to go to the location 2000h? a) MOV 2000h b) MOV A, 2000h **c) JMP 2000h** d) RET 2000h
7	What kind of a flag is the sign flag? a) General Purpose **b) Status** c) Address d) Instruction
8	The number of sign bits in a 32-bit IEEE format _____ **a) 1** b) 11 c) 9 d) 23
9	New CPU whose instruction set includes the instruction set of its predecessor CPU is said to be _____ with its predecessor. a) fully compatible b) forward compatible c) compatible **d) backward compatible**
10	A multiplexer of 2^n inputs has A. n-1 selection lines **B. n selection lines** C. n+1 selection lines D. 2^n selection lines
11	Binary numbers are stored in groups of flip flops called A. buses **B. registers** C. latches D. MOSFETs
12	A device that selects one of several analog or digital input signals and forwards the selected input into a single line is called A. multiplier **B. multiplexer** C. divider D. demultiplexer
13	The outputs of each register are a bundle of wires called **A. buses** B. flip flops C. latches

	D. MOSFETs
14	If $(101.01)_2=(x)_{10}$, then what is the value of x? a) 505.05 b) 10.101 c) 101.01 **d) 5.25**
15	If 0<E<255, then which of the following statement is true about X? a) Fractional number b) Infinity **c) Mixed number** d) Zero
16	The numbers written to the power of 10 in the representation of decimal numbers are called as _____ a) Height factors b) Size factors **c) Scale factors** d) None of the mentioned
17	If the decimal point is placed to the right of the first significant digit, then the number is called _____ a) Orthogonal **b) Normalized** c) Determinate d) None of the mentioned
18	_____ constitute the representation of the floating number. a) Sign b) Significant digits c) Scale factor **d) All of the mentioned**
19	The sign followed by the string of digits is called as _____ a) Significant b) Determinant **c) Mantissa** d) Exponent
20	In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits. a) 24 **b) 23** c) 20 d) 16
21	The normalized representation of $0.0010110 * 2_9$ is _____ a) 0 10001000 0010110 **b) 0 10000101 0110** c) 0 10101010 1110 d) 0 11110100 11100
22	The 32 bit representation of the decimal number is called as _____ a) Double-precision **b) Single-precision** c) Extended format d) None of the mentioned

23	In 32 bit representation the scale factor as a range of _____ **a) -128 to 127** b) -256 to 255 c) 0 to 255 d) None of the mentioned
24	In double precision format, the size of the mantissa is _____ a) 32 bit **b) 52 bit** c) 64 bit d) 72 bit
25	Which operations are used for addition, subtraction, increment, decrement and complement function: a. Bus b. Memory transfer c. Arithmetic operation d. **All of these**
26	In which transfer the computer register are indicated in capital letters for depicting its function: a) Memory transfer b) **Register transfer** c) Bus transfer d) None of these
27	The register that includes the address of the memory unit is termed as the ____: **a. MAR** b. PC c. IR d. None of these
28	The register for the program counter is signified as_____: **a.** MAR **b. PC** c. IR d. None of these
29	How many types of micro operations: a. 2 **b. 4** c. 6 d. 8
30	Which are the operation that a computer performs on data that put in register: a. Register transfer b. Arithmetic c. Logical **d. All of these**
31	Which micro operations carry information from one register to another: **a. Register transfer** b. Arithmetic c. Logical d. All of these
32	Micro operation is shown as: a. R1->R2

	b. R1<-R2 c. Both d. None
33	In memory transfer location address is supplied by____ that puts this on address bus: a. ALU **b. CPU** c. MAR d. MDR
34	Arithmetic operation are carried by such micro operation on stored numeric data available in_____: **a. Register** b. Data c. Both d. None
35	In arithmetic operation numbers of register and the circuits for addition at _____: **a. ALU** b. MAR c. Both d. None
36	Which operation are implemented using a binary counter or combinational circuit: a. Register transfer **b. Arithmetic** c. Logical d. All of these
37	Which operation are binary type, and are performed on bits string that is placed in register: **a. Logical micro operation** b. Arithmetic micro operation c. Both d. None
38	A micro operation every bit of a register is a: a. Constant **b. Variable** c. Both d. None
39	Which operation is extremely useful in serial transfer of data: a. Logical micro operation b. Arithmetic micro operation **c. Shift micro operation** d. None of these
40	IR stands for: a. Input representation **b. Intermediate representation** c. Both d. None
41	Which language specifies a digital system which uses specified notation: **a. Register transfer** b. Arithmetic

	c. Logical d. All of these
42	In register transfer which system is a sequential logic system in which flip-flops and gates are constructed: **a. Digital system** b. Register c. Data d. None
43	A counter is incremented by one and memory unit is considered as a collection of _____: a. Transfer register **b. Storage register** c. RTL d. All of these
44	Which is the straight forward register transfer the data from register to another register temporarily: a. Digital system b. Register c. Data **d. Register transfer operations**
45	Register are assumed to use positive-edge-triggered _____: **a. Flip-flop** b. Logics c. Circuit d. Operation
46	The memory bus is also referred as_____: **a. Data bus** b. Address bus c. Memory bus d. All of these
47	How many parts of memory bus: **a. 2** b. 3 c. 5 d. 6
48	In 3 state gate two states act as signals equal to: a. Logic 0 b. Logic 1 c. None of these **d. Both a & b**
49	every bit of register has: a. 2 common line b. 3 common line **c. 1 common line** d. none of these
50	Which operation refer bitwise manipulation of contents of register: **a. Logical micro operation** b. Arithmetic micro operation c. Shift micro operation d. None of these

	Unit 6: Processor Logic Design
1	Which symbol will be used to denote an micro operation: a. (^) **b. (v)** c. Both d. None
2	which symbol will be denote an AND micro operation: **a. (^)** b. (v) c. Both d. None
3	Which operation are associated with serial transfer of data: a. Logical micro operation b. Arithmetic micro operation **c. Shift micro operation** d. None of these
4	The bits are shifted and the first flip-flop receives its binary information from the_____: a. Serial output **b. Serial input** c. Both d. None
5	How many types of shift micro operation: a. 2 b. 4 **c. 6** d. 8
6	Which shift is a shift micro operation which is used to shift a signed binary number to the left or right: a. Logical **b. Arithmetic** c. Both d. None of these
7	which shift is used for signed binary number: a. Logical **b. Arithmetic** c. Both d. None of these
8	which shift is used for signed binary number: a. Logical **b. Arithmetic** c. Both d. None of these
9	The variable of_____ correspond to hardware register: a. RAM **b. RTL** c. ALU d. MAR

10	In which shift is used to divide a signed number by two: a. Logical right-shift **b. Arithmetic right shift** c. Logical left shift d. Arithmetic left shift
11	The external system bus architecture is created using from _____ architecture: a. Pascal b. Dennis Ritchie c. Charles Babbage **d. Von Neumann**
12	The network of wires or electronic path ways on mother board back side: a. PCB b. BUS **c. BOTH A and B** d. None of these
13	Which bus carry addresses: a. System bus **b. Address bus** c. Control bus d. Data bus
14	A 16 bit address bus can generate___ addresses: a. 32767 b. 25652 **c. 65536** d. none of these
15	CPU can read & write data by using : a. Control bus **b. Data bus** c. Address bus d. None of these
16	Which bus transfer singles from the CPU to external device and others that carry singles from external device to the CPU: **a. Control bus** b. Data bus c. Address bus d. None of these
17	When memory read or I/O read are active data is to the processor : **a. Input** b. Output c. Processor d. None of these
18	When memory write or I/O read are active data is from the processor: a. Input **b. Output** c. Processor d. None of these
19	Each memory location has: a. Address b. Contents **c. Both A and B**

	d. None of these
20	Customized ROMS are called: **a. Mask ROM** b. Flash ROM c. EPROM d. None of these
21	Which is the type of microcomputer memory: a. Processor memory b. Primary memory c. Secondary memory **d. All of these**
22	Which bus plays a crucial role in I/O: a. System bus **b. Control bus** c. Address bus d. Both A and B
23	Which register is connected to the memory by way of the address bus: **a. MAR** b. MDR c. SAM d. None of these
24	How many bit of MAR register: a. 8-bit **b. 16-bit** c. 32-bit d. 64-bit
25	Which are the READ operation can in simple steps: a. Address b. Data c. Control **d. All of these**
26	The information on the data bus is transferred to the _____register: a. MOC **b. MDR** c. VAM d. CPU
27	The lower red curvy arrow show that CPU places the address extracted from the memory location on the_____: **a. Address bus** b. System bus c. Control bus d. Data bus
28	The CPU sends out a ____ signal to indicate that valid data is available on the data bus: a. Read **b. Write** c. Both A and B d. None of these
29	The ____ place the data from a register onto the data bus: **a. CPU**

	b. ALU c. Both A and B d. None of these
30	The CPU removes the ___ signal to complete the memory write operation: **a. Read** b. Write c. Both A and B d. None of these
31	DS Stand for: **a. Data segment** b. Direct segment c. Declare segment d. Divide segment
32	IP Stand for: **a. Instruction pointer** b. Instruction purpose c. Instruction paints d. None of these
33	How many bits the instruction pointer is wide: **a. 16 bit** b. 32 bit c. 64 bit d. 128 bit
34	AD stand for: **a. Address data** b. Address delete c. Address date d. Address deal
35	PC stand for: **a. program counter** b. project counter c. protect counter d. planning counter
36	Which are the categorized of flag: a. Conditional flag b. Control flag **c. Both a and b** d. None of these
37	Which are the factor of cache memory: a. Architecture of the microprocessor b. Properties of the programs being executed c. Size organization of the cache **d. All of these**
38	The parity bits are used to check that a_____: a. Two bit error **b. Single bit error** c. Multi bit error d. None of these
39	Which causes the microprocessor to immediately terminate its present activity: **a. RESET signal**

	b. INTERUPT signal c. Both d. None of these
40	RD stands for: **a. Read** b. Register c. Request d. Real
41	DMA stands for: a. Direct memory allocation **b. Direct memory access** c. Direct memory application d. Direct memory acknowledgment
42	In which the processor uses a protection of the memory address to represent I/O ports: **a. Memory mapped I/O** b. I/O memory mapped c. Both a and b d. None of these
43	Which is the components of computer: a. System Bus b. CPU c. Memory Unit **d. All of these**
44	Which is the parts of memory unit: a. Processor memory b. Main memory c. Secondary memory **d. All of these**
45	A computer which has the microprocessor as_____ is called as a microcomputer: **a. CPU** b. ALU c. RU d. None of these
46	How can we make computers work faster? **a. The fetch-execute cycle and pipelining** b. The assembly c. Both A and B d. None of these
47	Which process information at a much faster rate than it can retrieve it from memory: a. ALU b. Processor c. Microprocessor **d. CPU**
48	The fetch-execute cycle is to use a system know as: a. Assembly line **b. Pipelining** c. Cache d. None of these

49	Who is the determined by the time taken by the stages the requires the most processing time: **a. Clock period** b. Flow through c. Throughput d. None of these
50	ISA stands for: a. Instruct set area **b. Instruction set architecture** c. Both a and b d. None of these